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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/023,235
Filing Date: December 17, 2001
Appellant(s): BERNSTEIN ET AL.

Pamela M. Riley
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3rd January 2008 appealing from the Office action mailed 28th June 2008 followed by Advisory Action mailed 12th September 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

U.S. Patent No. 6269277 issued to Hershenson et al

U.S. Patent No. 5,966,527 Krivokapic et al

U.S. Patent No. 6,028,994 issued to Peng et al

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112, first paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 1-3, 5-11, 13-22, 24-42 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Claims disclose generating computer model based on a target model where the target model is created using the performance parameters – the disclosure lacks enablement for creating such a computer model effectively based on performance parameters, which is critical or essential to the practice of the invention, but included in the claim(s) is not enabled by the disclosure.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the appellant regards as his invention.

2. Claim 1-3, 5-11, 13-22, 24-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appellant regards as the invention.

Regarding Claim 1-3, 5-11, 13-22, 24-42

Independent claims 1, 9, 14, 19, 24, 36 and 40 disclose limitation “first bound range” and “second bound range” for a “performance parameter”. However no specific

ranges are provided for this claim thereby failing to provide for the metes and bound for the ranges.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Appellant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. **Claims 1-27 & 30-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277hereafter) in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of appellant's own admission.**

Regarding Claim 1

HE'277 teaches a simulator (HE'277: Col.4 Lines 61-Col.5 Line 6) comprising:

a memory for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component (HE'277: Col.6 Lines 58-62 – a transistor) and has at least one performance attribute (HE'277: Col.3 Line 67 – Col.4 Line 5; Col.1 Lines 10-15); wherein the said computer model is generated based on the target model for said device (HE'277: Col.6 Lines 58-62) and wherein said target model is create using performance parameter ranges for the said performance attribute (HE'277: Col.5 Lines 40-46; Also see ranges in KR'527 Fig.1 Elements 103-107). The transistor models are posynomial models, which are created (optimized) for one or more performance specifications (HE'277: Col.6 Lines 3-6). HE'277 further teaches, said target model is adapted to determine the said target performance parameter range of said device (HE'277: Col.5 Lines 27-35; Col.6 Lines 1-48; Also See KR'527 – Fig.1 element 109). HE'277 teaches a processor in communication with the said memory and adapted to execute said computer model (HE'277: Col.4 Lines 61-Col.5 Line 6; Col.6 Lines 58-67).

HE'277 teaches target performance parameter range comprises multiple first bounded range (due to process variation being modeled as inequalities - HE'277 –

single variation as function f_o and multiple variations as f_i - Col.7 Line 1-59; Col.20 Lines 6-21, Col.21 Lines 10-34; specially see Col.20 Lines 35-41) and a second bounded range as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches each of said first bounded ranges comprises performance parameters variations due to manufacturing process variations and is based on a corresponding one of the multiple model curves for different designs of said device that achieves a same performance point (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-60; Also See Col.20 Lines 27-60; performance point Col.21 Lines 35-49) and; HE'277 teaches said second bounded range comprises performance parameters variations between designs for said design device (HE'277: Col.11 Lines 40-Col.12 Line16) as variations in at least the Length and Width of the transistor.

HE'277 teaches each of the multiple different designs is directed to a variation of a single design for the said integrated circuit, as variation is topology to optimize various parameters (HE'277: Col.6 Lines 1-24). The second bound range is constrained by these curves.

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process where the performance parameter are current voltage switch point (See claim interpretation), although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided (Abstract: Lines 19-27; Col.8 Lines 50-63).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes **[nature of problem being solved]** (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277 discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9-55).

Further appellant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example**, as is known in the art,** numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to ***predictively examine*** possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 2

HE'277 teaches that multiple designs are directed to variations of a single design (HE'277: Col.11 Lines 40-Col.12 Line16). For example changing the width (W) and lengths (L) of the transistors. These Length and Widths are constrained by most (Lmin, Wmin) and least linear (Lmax,Wmax) model curves.

Also See KR'527 Fig.1, wherein the element 110 has 4 points, two of them corresponding to process parameter variations making a bounded range and the other two related to lengths (design parameter).

Regarding Claim 3

HE'277 does not explicitly teach performance parameter *range* is the same for a target model of said device and a final hardware design of said device as the (performance) parameters are used for manufacturing and modeling. HE'277 also does not teaches interaction between the actual manufacturing and model simulation.

KR'527 teaches that performance parameter *range* is the same for a target model of said device and a final hardware design of said device (KR'527: Fig.6a, Fig.3) as the (performance) parameters are used for manufacturing and modeling.

KR'527 teaches in interaction between the actual manufacturing and model simulation (KR'527: Col.9-11).

Regarding Claim 5-7

HE'277 teaches using multiple constraints where the constraints vary as defined in the simulation, further HE'277 teaches performing tradeoff optimization between various constraints graphically displayed as curves (HE'277: Col.6 Lines 3-24). KR'527 also teaches statistical Monte Carlo based inputs (as ranges) & range correction (KR'527: Fig.6b, Col.12 Lines 8-50). Plurality of performance points (range) are selected as various input parameter values from statistical distributions mentioned above. Multiple first bound ranges can be seen in (KR'527: Fig.1) as well.

Regarding Claim 8

HE'277 teaches using geometric programming with its advantageous ability to solve thousands of constraints (HE'277: Col.5 Lines 6-35). Further, HE'277 teaches these constraints can be displayed as tradeoff (implying at least two constraints with plurality of evaluated results) in form of curve representing target performance parameters range with two-dimensional range of plurality of performance points (HE'277: Col.6 Lines 3-24; Also see KR'527: Col.12 Line 63-Col.13 Line 23).

Regarding Claim 9

Method claim 9 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 10

Method claim 10 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 11

Method claim 11 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 13

Method claim 13 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 14 & 15

Method claims 14 & 15 disclose similar limitations as claim 1 and are rejected for the same reasons as claim 1.

Limitation disclosed as “design goals” is further disclosed as “performance parameter”. HE’277 teaches producing a target model (HE’277: Col.4 Lines 61-67). Further, KR’527 teaches developing a device and product based on the target model (KR’527: Fig.6a, Col.9-11 Section III). The goals for device and product are interpreted as same goal, as indicated in the preamble “a product comprising a device” shows that product only has one device. Although “comprising” does not limited the scope, design goals can be seen in HE’277 (Col.6 Lines 1-24).

KR’527 teaches target performance comprises plurality of performance points as points in the V/I curves (KR’527: Fig. 6c, Also see Fig.1 element 110). Further by

appellant's disclosure, the tools to predict process and design variations are known in the art (Specification: [0033]).

Regarding Claim 16

Method claim 16 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 17

Method claim 17 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 18

Method claim 18 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 19

Method claim 19 discloses similar limitations as updated claim 1 and is rejected for the same reasons as claim 1.

KR'527 teaches developing a design for the device based on the target model (in simulator) (KR'527: Fig. 6a). KR'527 further teaches modifications to design wherein modification comprises modifying a particular feature and adding a particular feature of the design (KR'527: Col.6 Lines 34-59). KR'527 teaches determining primary parameters for a particular feature; determining secondary parameters from the said primary parameters (KR'527: at least in Col.2 Lines 51-63; also in Fig.6a-b-c-element 680-615-618; Col.13 Lines 10-23 – I/V curve from L, T, N parameters).

KR'527: Col.2 Lines 51-63 states:

> Before an accurate model of semiconductor device 200 may be obtained, certain "parameters" must be extracted from semiconductor device 200, as illustrated in FIG. 1. Typically, a device simulator requires specific device "parameters" in order to provide a simulation. For example, one semiconductor device simulator requires five specific sets of parameters, as illustrated by parameters 103-107. Some of the parameters are extracted from device parameter extractor 102. Some of these parameters may correspond to physical measurements of transistor device 200, such as channel length L and doping concentration N+ ***[Primary parameters]***, while other parameters may be based on or derived from these physical measurements or other parameters ***[secondary parameters]***.

KR'527 teaches determining secondary parameters from said primary parameters (KR'527: Fig.6a-b-c; Col.13 Lines 10-23 – I/V curve from L, T, N parameters) where the primary parameters are inputted into process simulator and secondary parameters are derived from primary parameters (element 680-615-618) and inputted into device simulator (Element 640).

KR'527 teaches balancing choices (KR'527: Col.2 Lines 20-24, Col.4 Lines 30-34) related to modification and particularly to primary and secondary parameters (KR'527: Fig.6a-b-c; Col.13 Lines 10-23 – I/V curve from L, T, N parameters; element 680-615-618) so that target performance parameters will remain within first bound range and second bound range (KR'527: Abstract: Lines 19-27; Col.8 Lines 50-63).

Regarding Claim 20

KR'527 teaches correlating secondary parameters to at least one further secondary parameter (Col.2 Lines 51-63; Col.12 Lines 8-62; Fig.6a-c & 7 a-c).

Regarding Claim 21

KR'527 teaches verifying that all primary and secondary parameters are within allowable limits (Col.13 Lines 24-62).

Regarding Claim 22

HE'277 teaches specifying parameters as first order and second order (HE'277: Col.11 Line 59-Col.12 Line 15).

Regarding Claim 24

HE'277 teaches a method of developing a product (HE'277: Col.4 Lines 61-Col.5 Line 6) comprising a device with at least one performance attribute (HE'277: Col.3 Line 67 – Col.4 Line 5; Col.1 Lines 10-15) wherein the said device comprises a integrated circuit component (HE'277: Col.6 Lines 58-62 – as transistor) and wherein said target model is create using performance parameter for the said performance attribute (HE'277: Col.5 Lines 40-46). The goals for device are based on the product – i.e. size of the transistors is dependent on the goal of the amplified in HE'277 (HE'277: Col.6 Lines 1-24). HE'277 teaches target performance parameter range includes a multiple first bounded range (due to process variation being modeled as inequalities - HE'277: Col.20 Lines 6-21, Col.21 Lines 10-34; Also see ranges in KR'527 Fig.1 Elements 103-107) and a second bounded range as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches target performance parameter range comprises multiple first bounded range

(due to process variation being modeled as inequalities - HE'277 – single variation as function f_o and multiple variations as f_i - Col.7 Line 1-59; Col.20 Lines 6-21, Col.21 Lines 10-34; specially see Col.20 Lines 35-41) and a second bounded range as inequality constraints (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48). The Circuit topologies pointed out further for more complex elements e.g. (herein the product built from the device HE'277 Col.5 Lines 50-51) are based on the selection of one of designs of the transistors ranging from simple to complex. When the topologies are optimized a design is selected based on the required performance parameters (HE'277: Col.6 Lines 21-35). HE'277 teaches each of said first bounded ranges comprises performance parameters variations due to manufacturing process variations and is based on a corresponding one of the multiple model curves for different designs of said device that achieves a same performance point (HE'277: Col.20 Lines 6-21, Col.21 Lines 10-60; Also See Col.20 Lines 27-60; performance point Col.21 Lines 35-49) and; HE'277 teaches said second bounded range comprises performance parameters variations between designs for said design device (HE'277: Col.11 Lines 40-Col.12 Line16) as variations in at least the Length and Width of the transistor.

HE'277 teaches each of the multiple different designs is directed to a variation of a single design for the said integrated circuit, as variation is topology to optimize various parameters (HE'277: Col.6 Lines 1-24). The second bound range is contrainted by these curves.

HE'277 does not teach explicitly first bounded range comprising performance parameter variations within a single manufacturing process *where the performance parameter are current voltage switch point*, although HE'277 discloses generation of appropriate device model based on the technology, process performance parameters.

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided as V/I Curves (Abstract: Lines 19-27; Col.8 Lines 50-63). The simulator simulates the computer model, created in the simulator, of the said product to determine if the product/device goals are met (KR'527: Fig.6a-6c).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of KR'527 to HE'277 to design a simulation system coupled with actual data for more realistic results. The motivation to combine would have been that HE'277 and KR'527 are analogous art modeling the device and process of semiconductor manufacturing processes **[nature of problem being solved]** (KR'527: Abstract; HE'277: Abstract), where the simulation is controlled by the multiple attributes/parameters/constraints (HE'277: Summary) inputted into the device & process simulator (KR'527: Fig4, 5a-b). HE'277 can further augment the device and process simulator of KR'527 as HE'277 discloses advanced simulator using genetic programming (HE'277: Col.3 Lines 9-55).

Further appellant had acknowledged such tools for predicting the outcome of design and process variations are known in the art (Specification: [0033])

> For example**, as is known in the art,** numerical finite-element simulation codes such as PISCES, FIELDAY, or DAMOCLES can be used to ***predictively examine*** possible device designs based on a spatially-discretized physical model of a transistor and adjusted physical and process assumptions.

Regarding Claim 25

Method claim 25 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 26

Method claim 26 discloses similar limitations as claim 4 and is rejected for the same reasons as claim 4.

Regarding Claim 27

KR'527 teaches the step of accepting altered device design further comprises the steps of carrying out experiments on test chips (KR'527: Fig.3, actual to simulated data comparison & guard band generation Col.13 Lines 32-62).

Regarding Claim 30

KR'527 teaches calculating a primary parameter from a physical device feature as L, T and N values (KR'527: Col.11 at least in Lines 19-27); correlating a secondary parameter from said primary parameter as associating resulting I/V curve with the L, T, N values (KR'527: Col.13 Lines 10-23); calculating secondary parameter based on the primary parameters based on predetermined primary to secondary correlation I/V curve based on L, T, and N value equation (KR'527: Col.13 Lines 10-23; Fig. 6c;

HE'277; Equation 16); and comparing said secondary parameter to said target performance parameter (KR'527: Col.13 Lines 24-37).

Regarding Claim 31

KR'527 teaches correlating other secondary parameters from correlations to said secondary parameters as correlating the V/I curve to the various channel length and attributes (short, short long etc) (KR'527: Fig 5a, Element 500).

Regarding Claim 32

KR'527 teaches primary parameter is directly related to physical device feature as related to channel length, doping, gate oxide thickness (KR'527: Col.11 at least in Lines 19-27 & Table C).

Regarding Claim 33

KR'527 teaches correlating primary to secondary parameters (KR'527: Fig 5a, Element 500). Secondary parameters could be derived parameters like "beta" whose derivation using equation is well known in the art.

Regarding Claim 34

Method claim 34 discloses similar limitations as claim 3 and is rejected for the same reasons as claim 3.

Regarding Claim 35

Method claim 35 discloses similar limitations as claim 6 and is rejected for the same reasons as claim 6.

Regarding Claim 36

Product claim 36 discloses similar limitations as updated claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product as alternate embodiment (HE'277: Col.22 Lines 1-21).

Regarding Claim 37

Product claim 37 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 38

Method claim 38 discloses similar limitations as claim 7 and is rejected for the same reasons as claim 7.

Regarding Claim 39

Method claim 39 discloses similar limitations as claim 8 and is rejected for the same reasons as claim 8.

Regarding Claim 40

Method claim 40 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches a computer program product (storage device) readable by computer and tangibly embodying a program of instructions executable by said computer to perform an integrated circuit development method (HE'277: Col.22 Lines 1-21).

Regarding Claim 41

HE'277 teaches that *multiple* designs are directed to variations of a single *design* (HE'277: Col.11 Lines 40-Col.12 Line16). For example changing the width (W) and

lengths (L) of the transistors. These Length and Widths are constrained by most (Lmin, Wmin) and least linear (Lmax,Wmax) model curves.

Also See KR'527 Fig.1, wherein the element 110 has 4 points, two of them corresponding to process parameter variations making a bounded range and the other two related to lengths (design parameter).

Regarding Claim 42

HE'277 teaches computer-implemented method (HE'277: Col.4 Lines 61-Col.5 Line 6) of developing a product comprising a device with at least one performance attribute (HE'277: Col.6 Lines 1-24), wherein said device comprises an integrated circuit component (HE'277: Col.6 Lines 58-62 – a transistor), said method comprising: designing said product using a computer model that is based on a target model of said device, wherein said target model is created using said a target performance parameter range for said performance attribute (HE'277: Col.6 Lines 1-24), wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range (HE'277: Col.5 Lines 27-35, 40-46; Also see ranges in KR'527 Fig.1 Elements 103-107), wherein each of said first bounded ranges comprises a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point, wherein each of said multiple different designs is directed to a variation of a single design for said device (due to process variation being modeled as inequalities - HE'277 – single variation as function f_o and multiple variations as f_j - Col.7 Line 1-

59; Col.20 Lines 6-21, Col.21 Lines 10-34; specially see Col.20 Lines 35-41, HE'277: Col.6 Lines 1-24), wherein said second bounded range is constrained is constrained (due to variation of multiple design in complexity for a transistor (or said device) - HE'277: Col.5 Lines 40-48) by a most linear of said multiple model curves mad a least linear of said multiple model curves (Also See KR'527: Fig.1 Element 110) and Wherein target performance parameter range is constrained by an upper edge of a first bounded range around said most linear of said multiple model curves and a lower edge of another first bound range around said least linear of said multiple model curves (Also See KR'527: Fig.1 Element 110).

Motivation to combine HE'277 with KR'527 is same as in claim 1.

4. **Claims 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6269277 issued to Hershenson et al (HE'277 hereafter), in view of U.S. Patent No. 5,966,527 Krivokapic et al (KR'527 hereafter), further in view of appellant's own admission, further in view of U.S. Patent No. 6,028,994 issued to Peng et al (PE'994 hereafter).**

Regarding Claim 28 & 29

Teaching of HE'277, KR'527 and appellant's own admission are shown in claim 24 rejections above.

HE'277 & KR'527 do not teach design goals for product, developing product fro from target model and product model simulation & alteration based on feedback.

PE'994 teaches teach design goals for product (PE'994: Col.2 Line 49-59 – predicted performance), developing product from target model as combined product

& device model represented by product performance model (PPM) (PE'994: Fig. 1; Col.6 Lines 57-67) and product model simulation & alteration based on feedback as self learning (PE'994: Fig.1 Step 64). The product is represented as package of wafer chip and the device is represented as wafer chip (PE'994: See Fig.1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of PE'994 to HE'277 & KR'527. The motivation to combine would have been that HE'277 & KR'527 and PE'994 are attempting to design a model that can mimic and or predict the performance of the semiconductor model (PE'994: Abstract; HE'277 & KR'527: Abstracts) based on the input parameters. Further, teaches PE'994 specifying the input parameters as ranges (PE'994: Fig.3 Col.5 Lines 35-48) for performance which is very similar to the KR'527 teachings disclosed before relating to ranges for performance parameters.

(10) Response to Argument

a. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

(1) Independent Claim(s) 1, 9, 14, 19, 24, 36, 40, 42

Examiner thanks appellant in explaining the technology and their interpretation of the claim in remarks on Pg.55-58, however the claim 1 states:

> "A simulator comprising:
> **a memory** for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute, wherein said **computer model is generated based on a target model** for said device and wherein **said target model is created using a *target performance parameter range*** for said performance attribute and is adapted to predict process and design variations of said device; **and a processor** in communication with said memory and **adapted to *determine said target performance parameter range* and to execute said computer model,…"**

As best understood the target model is created using the target performance parameter range (see memory step), and performance parameter range are determined using the computer model (see processor step) when executed by the processor. However computer model is generated based on the target model (see memory step), thereby presenting a *cyclical problem* in building/determining which one of the computer model, target model or performance parameter range is the starting point. Therefore it would not be possible to build the target model as claimed. This problem in building the model is not addressed by appellant. Further the disclosure fails to present details of either the computer model, target model or performance parameter range *for the device/integrated circuit component,* in the sections cited by the appellant (see specification [0023], [0025], [0026], 0035], [0036]). Hence one of ordinary skill in the art would be unable to *build and/or use the claimed invention*. For at least the reasons above examiner requests the rejection to

be maintained. Claims 9, 14, 19, 24, 36, 40, 42 present the same argument and are responded to in the same manner as above.

b. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

(1) Independent Claim(s) 1, 9, 14, 19, 24, 36, 40, 42

(Argument 1) Appellant has argued in Remarks Pg.58 -59:

> ….While no specific ranges are provided in the claims, none are required. **[1]** The range is application specific, as claimed. **[2]** That is, each first bounded range is a range of performance parameter variations due to manufacturing process variations and is based on a corresponding one of the model curves for different designs for the device that achieve a same performance point. Similarly, the second range is constrained by at least two of these curves so as to comprise performance parameter variations between multiple different designs for the device.
>
> Support for these ranges is found in paragraphs [0020]-[0030] of the published patent application and Figures 2-3 **[3]** …

(Response 1) Appellant's statement in **[1]** contradicts the following statement presented in **[2]**, as no range is presented in the claim and a specific application of modeling an integrated circuit/device/component is disclosed in the claim.

Further the examiner disagrees, that no specific range is required, as most of the claim is directed towards identifying the type of performance parameter (variations due to manufacturing process & device design). With so much emphasis on the performance parameter range, lack of metes and bounds makes the claim indefinite.

As per **[3],** contrary to as alleged by the appellant, none of the paragraphs [0020]-[0030] or Fig.2-3 specifically teach metes and bounds of the performance parameter range.

Appellant reiterates their argument on Pg.60-62 and repeats it for claims 9, 14, 19, 24, 36, 40, 42 which are responded to in the same manner as above.

c. REJECTIONS UNDER 35 U.S.C. § 103(A) BASED ON HERSHENSON AND KRIVOKAPIC

(1) Independent Claim(s) 1 and dependent claims 2-3 and 5-8

Appellant's summary of Hershenson & Krivokapic on Pg. 62-64 is noted.

(Argument 2) Appellant has argued in Remarks Pg.65:

> The final rejection of claim 1 does not address the feature in claim 1 that the *target model is adapted to predict both process and design variations of said device.*

(Response 2) First, this limitation is in the preamble and is intended use of the target model. Secondly, Hershenson teaches performance prediction (Hershenson: Col.5 Lines 65-Col.6 Line 13) based both on the process variation (Hershenson: Also see Col.21 Lines 19-28 - specifically addressing process variations; Col.20 Lines 6-21 where oxide thickness is process variation parameter) and design variation (Hershenson: Col.6 Lines 14-24 where topologies are design variation; Col.11 Lines 32-61 specifically Col.11 line 61 teaching design variation within a range of design parameters *L*ength(L*i*) and *W*idth (W*i*)) for a given model.

(Argument 3) Appellant has argued in Remarks Pg.65:

> The final rejection further provides that both Hershenson and Krivokapic disclose "wherein said target model is create using performance parameter ranges for said performance attribute (HE'277: Col. 5 Lines 40-46; Also see ranges in KR'527 Fig. 1 Elements 103-107)." The final rejection further provides that Hershenson and Krivokapic both disclose "said target model is adapted to determine the said target performance parameter range of said device (HE'277:Col. 5 Lines 27-35; Col 6 Lines 1- 48; Also See Kr'527-Fig.1 element 109). The Appellants respectfully disagree.
> Specifically, the claimed feature is "wherein said target model [for said device] is created using a target performance parameter range for said performance attribute [of said device]. It is not a target model that is created using performance parameter ranges for the performance attribute, nor is it a target model that is adapted to determine the target performance parameter range. **[1]**

(Response 3) As per [1], appellant merely alleges that the target model is not created using a target performance parameter *range*. Examiner respectfully disagrees with appellant. Hershenson Col.5 Line 62-Col.6 Line 24 states:

> After a transistor model has been selected, the next step in designing or optimizing a circuit is to select a circuit topology or a group of circuit topologies, step 52. A user then selects performance specifications for the desired device, such as an op-amp, step 54. The system generates a geometric program using posynomial or monomial expressions for the defined performance specifications, step 56. **[a]** The user can select one of three optimization modes. **[b]** The first mode is a standard optimization mode in which one or more performance specifications are optimized subject to a set of constraints. The second mode is a robust design mode in which in addition to the standard optimization there is an additional constraint that the design should work under several process conditions. The third mode is a trade-off curve mode. In this mode the optimization problem is repeatedly solved as the system sweeps over the range of selected constraint limits. **[c]** The output in this mode is a series of curves displaying the trade-offs of the different constraint values. For example, for an op-amp, a user can repeatedly minimize power as the system sweeps the value of the minimum required unity-gain bandwidth, and holds constant all the other constraints. The resulting curve shows the globally optimal trade-off between unity-gain bandwidth and power (for the values of the other limits). The system solves the geometric program to provide the desired results, step 60. The solution provided is the globally optimal solution for the defined performance specifications. If a user selected a group of circuit topologies the system can rapidly perform the optimization analysis on each circuit topology to select the optimal circuit topology.

As seen in [a], target model is optimized with performance specifications using mathematical posynomial and monomial expressions. Further [c] teaches evaluation [performance] constraints over a range. Further, posynomial and monomial expressions are range bounded as shown in Hershenson Col.21 Lines 19-54:

> "Process variation will change the open-loop gain, making it impossible to achieve a design that yields open-loop gain of exactly 80 dB for more than a few process parameter values. The solution to this problem is to convert such specifications into inequalities. The specification might, for example, be changed to require that the open-loop gain be more than 80 dB, or that it be between 80 dB and 85 dB. **[d]** Either way the robust problem now has at least a chance of being feasible.
> It's important to contrast a robust design for a set of process parameters A=[.alpha..sub.1, . . . , .alpha..sub.N] with the optimal designs for each process parameter. **[g]** The objective value for the robust design is worse (or no better than) the optimal design for each parameter value. This disadvantage is offset by the advantage that the design works for all the process parameter values.
> So far the case in which the set A is finite has been described. But in most real cases it is infinite; for example, individual parameters lie in ranges. **[e]** As described above, such situations can be modeled or approximated by sampling the interval. While this appears to always work in practice, it gives no guarantee, in general, that the design works for all values of the parameter in the given range; it only guarantees performance for the sampled values of the parameters.

> There are many cases, however, when the performance for a parameter value can be guaranteed in an interval. **[f]…"**

As can be seen from Hershenson Col.21 Lines 19-54 [d], [e] and [f] above a clear indication is present that ranges used as input to optimize the model.

(Argument 4) Appellant has argued in Remarks Pg.65:

> Furthermore, the target model features cited in the Office Action as being disclosed by the prior art references are, by definition mutually exclusive. That is, the model can either be created using the range or it can determine the range, but not both (i.e., you can not determine the range with the model, if you actually need it in order to create the model). **[1]** Also, even if for arguments sake, the Hershenson and Krivokapic both did teach a target model created using performance parameters ranges for a performance attribute, they do not go beyond that to teach the limiting feature in the present invention that the target model is created based on a single target performance parameter range for a given performance attribute as claimed. **[2]**

(Response 4) As per [1] appellant seems to be contradicting the claim language.

Repeated again for brevity, claim 1 states:

> "A simulator comprising:
> **a memory** for storing a computer model of an integrated circuit comprising a device that comprises an integrated circuit component and that has at least one performance attribute, wherein said **computer model is generated based on a target model** for said device and wherein **said target model is created using a *target performance parameter range*** for said performance attribute and is adapted to predict process and design variations of said device; **and a processor** in communication with said memory and **adapted to *determine said target performance parameter range* and to execute said computer model,…**
> wherein said target performance parameter range comprises multiple first bounded ranges and a second bounded range,"

As explained earlier, claim seem to indicate a cyclical trend where the target performance parameter range is used to create the target model, target model used to create computer model and computer model executed to determine the target performance parameter range. In plain meaning the target performance parameter range is input as well as output, where emphasis now is on the range.

Arguendo, even if the appellant argument is considered, Hershenson Col.21 Lines 19-54 teaches input as range and output as series or curves displaying the tradeoff of different constraint values in Hershenson Col.6 Lines 12-14, which are ranges.

This fact is elaborated on & Krivokapic (Abstract: Lines 13-16, Fig.1 and 6c showing I/V bounded curves). Please also see appellant's disclosure 2 & 3 in comparison to Fig.6c right bottom.

As per [2], appellant states "they [Hershenson & Krivokapic] do not go beyond that to teach the limiting feature in the present invention that the target model is created based on a ***single target performance parameter range*** for a given performance attribute as claimed." Examiner respectfully disagrees, as Col.5 Line 62-Col.6 Line 24 clearly teaches optimizing multiple [performance] constraint parameters. See in Response 3 above.

(Argument 5) Appellant has argued in Remarks Pg.66:

> "…But Hershenson does not teach or disclose that a target model for a device (which is a component of an integrated circuit) is created using a target performance parameter range for a given performance attribute of that device, much less that such a target model is subsequently used to generate a computer model of the integrated circuit."

(Response 5) Appellant is arguing a target model for a device (which is a component of an integrated circuit), contrary to claimed limitation where the device comprises an integrated circuit component (see claim 1 preamble).

In either case, Hershenson teaches a device as an operational amplifier (in short op-amp - Hershenson Col.5 Lines 62-67) and optimization of component performance constraints like length and width of transistor model (component) in the op-amp device (Hershenson: Col.11 Dimension Constraint section where the length and width of transistors are optimized as presented in range. see Eq.7 specifically).

(Argument 6) Appellant has argued in Remarks Pg.67:

> It [Krivokapic] does not create a target model for a device (which is a component of an integrated circuit) using a target performance parameter range for a given performance attribute of that device, much less that this target model is subsequently used to generate a computer model of the integrated circuit.

(Response 6) This teaching is mapped/presented in Hershenson. Secondly, Krivokapic also teaches using various values from the range to create and simulate the target model (See Krivokapic: Fig.1 & 3). Further, the rejection is made under 35 USC 103, using obviousness argument and appellant is performing piecemeal analysis.

(Argument 7) Appellant has argued in Remarks Pg.67-68:

> "…The Appellants submit that *a set of specifications* for *a set of values of parameters* necessarily does not *amount to the multiple bounded first bounded ranges* included in the target performance parameter range of the claimed invention."

(Response 7) First bounded ranges are taught by Hershenson Col.21 Lines 19-54. See Response 3 for detailed response and highlighted teachings of Hershenson. The first bound range represents, range of performance parameter variations due to manufacturing process which is taught by Hershenson Col.21 Lines 19-54. See Response 3 underlined section **[g]** from teaching of Hershenson Col.21 Lines 19-54.

(Argument 8) Appellant has argued in Remarks Pg.68:

> Additionally, the referred to values of parameters (e.g., transistor threshold voltages, mobilities, oxide parameters, channel modulations parameters, supply voltages, and load capacitances) correspond to specifications for a circuit and not to the specifications for a device (e.g., a transistor) that is incorporated into the circuit, as in the present invention.

(Response 8) Appellant is alleging values of parameters, e.g. transistor threshold voltages, mobilities, oxide parameters, channel modulations parameters, supply voltages correspond to specification for a circuit and not specification for a device like transistor. Appellant is incorrect, e.g. transistor threshold voltages is the voltage when transistor would turn on. Similarly [electron] mobilities, [gate oxide] oxide parameters, [CMOS] channel modulations parameters are parameters associated with MOS transistor. Circuit parameters are for the circuit built by transistor components e.g. an

operational amplifier (op-amp) having parameters like open loop gain 3dB bandwidth (Hershenson: Col.10 Lines 48-Col.11 Line 30).

(Argument 9) Appellant has argued in Remarks Pg.68:

> Thus, Hershenson does not teach or suggest that the target model for a device within an integrated circuit is created using a target performance parameter range for a performance attribute of the device, much less that this target performance parameter range of the device's performance attribute comprises "multiple first bounded ranges".

(Response 9) Examiner respectfully disagrees, Hershenson teaches that the target model for a device (e.g. transistor – Hershenson Col.11 Lines 40 –Col.12 Lines 55) within an integrated circuit (e.g. operational amplifier Fig.3 having MOS transistors) is created using a target performance parameter range for a performance attribute of the device (Col.5 Lines 61-Col6 Lines 36). Response 3 & 4 disclose in detail mapping for first bounded range.

(Argument 10) Appellant has argued in Remarks Pg.69:

> Hershenson does not teach or suggest that the target model for a device (i.e., for a component of the integrated circuit) is created using a target performance parameter range for a performance attribute of the device, much less that the target performance parameter range of the device's performance attribute comprises both "multiple first bounded ranges" and "a second bound range".

(Response 10) Appellant alleges that target model of device (transistor) is not created using target performance parameter range, and Hershenson teaches only after selecting the transistor model to select from topologies (various designs) and performance specification (Hershenson: Col.5 Lines 61-Col6 Lines 36). Appellant is merely arguing the limitation without providing how this is different than what is claimed. There is no disclosure present that teaches specifically how a target model of device is created using target performance parameter range.

As for second bound range represents performance parameter variations between multiple different designs for the device which is taught by Hershenson (Col.5 Lines 61-Col6 Lines 36) as topologies and also maps the output of simulation based on these topologies.

(Argument 11) Appellant has argued in Remarks Pg.69:

> As discussed above, Hershenson at col. 20, line 6-col. 21, line 67, discusses a method of developing circuit designs that meet a set of specifications for a set of values of parameters. "The basic idea is to list a set of possible parameters, and to replicate design constraints for all possible parameter values" (see col. 20, lines 13-15). Nothing in the cited portion of Hershenson indicates that each one of multiple first bounded ranges comprises "a range of performance parameter variations due to manufacturing process variations", **[1]** much less that each one is "based on a corresponding one of multiple model curves for different designs of said device that achieve a same performance point."**[2]**

(Response 11) As per [1], please see Hershenson Col.20 Lines 5-Col.21 line 51 at least. Both the design and (manufacturing) process parameters are varied (Col.20 Lines 22-34) to achieve a performance point (Col.21 Lined 19-27) within a specified range.

As per [2], design parameters are also varied (as shown in response to [1] above and Col.11 Lines 40-66) to achieve a common goal for a performance point. e.g. 80-85 dB open loop gain on an operation amplifier (Col.21 Lined 19-27).

(Argument 12) Appellant has argued in Remarks Pg.70:

> Nothing in the cited portion of Hershenson teaches or discloses that the system uses multiple different designs for the device that are directed to a variation of a single design for the integrated circuit, rather as set out above only a single transistor model is selected and the integrated circuit design is optimized in light of that transistor model selection.

(Response 12) Hershenson states using multiple topologies which are multiple designs as in Col.6 Lines 20-24:

> The solution provided is the globally optimal solution for the defined performance specifications. If a user selected a group of circuit topologies [designs] the system can rapidly perform the optimization analysis on each circuit.

(Argument 13) Appellant has argued in Remarks Pg.70:

> It is unclear what the Examiner is referring to by the statement "The second bounded range is constrained by these curves." Nothing in the cited portion of Hershenson (i.e., col. 6, lines 1-24) teaches or discloses multiple model curves, much less that a second bounded range of a target performance parameter range **[1]**of a performance attribute of a device in an integrated circuit is constrained by "at least two of said multiple model curves so as to comprise performance parameter variations between said multiple different designs for said device." **[2]**

(Response 13) As per [1], The second bounded range is device parameters (col. 6, lines 1-24) based on topologies, and further design features as length and width of the transistors (Col.11 Lines 32-66). The length and width, min and max values disclosed on the Col.11 Eq.7 determine the current in the various equations 9, 10 and 11. These current biases having lower and upper bounds can be used in geometric programming (model) (Col.12 Lines 57-63). These lower and upper ranges represent a bounded range for voltages (Col.12 Line 64- Col.15 Line 25).

As per [2], for multiple model curves, these are evident from Krivokapic (Abstract, Fig.1, Fig.3 element 307, Fig.6c) showing current-voltage curves, based on device simulator (Fig.6c Element 640) and design parameters (Fig.3 element 306).

No new arguments are presented for dependent claims 2-3 and 5-8.

(2) Independent Claim(s) 9 and dependent claims 10-11 and 13

(Argument 14) Appellant has argued in Remarks Pg.71-72:

> Furthermore, the Appellants submit that the cited prior art references do not teach the additional feature in independent claim 9 of "designing said product using a computer model that is based on a target model of said device, wherein said target model is created using a target performance parameter range for said performance attribute;" The final rejection of claim 9 does not address each of the claimed features but rather refers to the rejection of claim 1. However, claim 1 does not include a "designing" limitation and, thus, the rejection of claim 1 does not address the feature designing said product (which has a device comprising an integrated circuit component) using a computer model that is based on a target model of said device.

(Response 14) The system in claim 1 includes memory and processor to execute model stored in the memory. This limitation is mapped to Hershenson Col.6 Lines 49-52. This limitation also teaches designing a product to perform the function of the claim 1. Remaining arguments presented for claim 9 are responded to in the same manner as claim 1. No new arguments are presented for dependent claims 10-11 and 13.

(3) Independent Claim(s) 14 and dependent claims 15-18

(Argument 15) Appellant has argued in Remarks Pg.73:

> Specifically, as discussed above, Krivokapic teaches a method of modeling the behavior of a mass-produced device (e.g., a transistor) to determine statistical worst case curves and predict the behavior of a device manufactured on a processing line. It does not teach developing a device and product based on a target model. **[1]** Furthermore, the Appellants submit that the product and the device, as claimed, are separate and distinct patentable features as are the product goals and the device goals. **[2]** The fact that the preamble refers to a "product comprising a device" does not limit the invention to a product having only one device. The subsequent claim language clearly indicates that the product and device are separate and distinct from each other in that the product, only after the target model for the device is produced, is designed with the device based on the target model. **[3]** If the product and the device were interpreted as being the same thing, there would be no need to design the product after producing the target model for the device. Similarly, if the device goals and product goals were interpreted as the same goals, then there would be no need to develop device goals based on product goals.

(Response 15) As per [1], Hershenson is used to show device model based on the performance parameters (constraints bounded by ranges in Col.11 Line 31-Col.14 Line 25, specifically eq.7). Further the model is used to construct a product (Hershenson: e.g. operational amplifier Col.6 Lines 13-24; Krivokapic Fig.6a Col.9-11 – showing modeling of semiconductor process and device like operational amplifier – specifically Col.10 Lines 53-58).

As per [2], the product goal is optimization performed for the operational amplifier (Hershenson: Col.10 Lines 48-Col.11 Line 30), and device goal optimization is

performed on the transistor (Hershenson: Col.11 Lines 40-Line 66; Col.20 Lines 7-67 at least).

As per [3], appellant merely alleges the distinction, and fails to specifically point to which claim the argument applies. No new arguments are presented for dependent claims 15-18.

Remaining arguments presented for claim 14 are responded to in the same manner as claim 1.

(4) Independent Claim(s) 19 and dependent claims 20-22

Appellant merely alleges that the limitations in claim 19 are not taught. Remaining arguments presented for claim 19 are responded to in the same manner as claim 1.

No new arguments are presented for dependent claims 20-22.

(5) Independent Claim(s) 24 and dependent claims 25-35

(Argument 16) Appellant has argued in Remarks Pg.75:

> The Appellants also respectfully submit that, for the same reasons cited above in paragraph VII.A.2.c.(3) with regard to independent claim 3, the cited prior art references do not teach the additional features in independent claim 24 of "developing device goals for said device, wherein said device goals are based on product goals."

(Response 16) The product goal is optimization performed for the operational amplifier (Col.10 Lines 48-Col.11 Line 30), and device goal optimization is performed on the transistor (Col.11 Lines 40-Line 66; Col.20 Lines 7-67 at least).

Appellant merely alleges that the limitations in claim 24 are not taught. Remaining arguments presented for claim 24 are responded to in the same manner as claim 1.

No new arguments are presented for dependent claims 25-25.

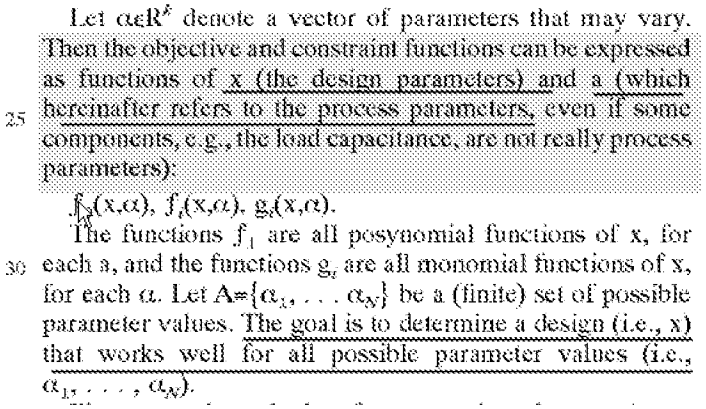
(6) Independent Claim(s) 36 and dependent claims 37-38

(Argument 17) Appellant has argued in Remarks Pg.75-76:

> "The Appellants also respectfully submit that the cited prior art references do not teach the additional feature in independent claim 36 of "a set of subroutines **[1]** created using a target performance parameter range for said performance attribute, wherein said set of subroutines, when executed by said computer predict process and design variations of said device." … As mentioned above, the final rejection of claim 1 does not address predicting both process and design variations of said device. **[2]**The only other information provided in the final rejection of claim 36 relates to the fact that Hershenson which indicates that the invention of Hershenson can be implemented as a computer program product.

(Response 17) As per [1], examiner disagrees with appellant, as set of subroutines is a program product to be statutory, which is taught by Hershenson Col.22 Lines 1-21.

As per [2], Please see Response 2 above and also Hershenson Col.20 Lines 22-27 stating:



Let $\alpha \in R^k$ denote a vector of parameters that may vary. Then the objective and constraint functions can be expressed as functions of x (the design parameters) and a (which hereinafter refers to the process parameters, even if some components, e.g., the load capacitance, are not really process parameters):

$f_0(x,\alpha)$, $f_i(x,\alpha)$, $g_i(x,\alpha)$.

The functions f_i are all posynomial functions of x, for each a, and the functions g_i are all monomial functions of x, for each α. Let $A=\{\alpha_1, \ldots \alpha_N\}$ be a (finite) set of possible parameter values. The goal is to determine a design (i.e., x) that works well for all possible parameter values (i.e., $\alpha_1, \ldots, \alpha_N$).

No new arguments are presented for dependent claims 37-38.

(7) Independent Claim(s) 40 and dependent claims 41

No new arguments are presented for claim 40 other than the ones already presented and addressed in Response 1-13 (for claim 1), 15 (for claim 14) and 16 (for claim 24). No new arguments are presented for dependent claim 41.

(8) Independent Claim(s) 42

No new arguments are presented for claim 42 other than the ones already presented and addressed in Response 1-13 (for claim 1).

d. CLAIM INTERPRETATION

(Argument 18) Appellant has argued in Remarks Pg.78:

> Regarding the term "performance parameter", the Appellants submit that performance parameter and performance attribute, as defined in the specification, are not limited to a "current voltage switch-point" of a transistor computer model. **[1]** Rather as discussed in paragraph [0017]- [0018], "the invention is also applicable to any component of any product, where the performance attributes of that component "help determine the functionality of the integrated product. Examples, include chemical components and subcomponents of drugs, or the insole of a shoe, or the foam insulator of a hot tub. In each example, the former is the "device" and the latter is the "product"." **[2]**

(Response 18) As per [1], examiner is rejecting one embodiment of the "performance parameter" as defined by the specification [0018].

As per [2], examiner does not see how the product could be chemical components and subcomponents of drugs, or the insole of a shoe, or the foam insulator of a hot tub, when the claim is specifically directed towards model of an integrated circuit and system, method and program product thereof. Appellant has provided no basis for this argument.

(Argument 18) Appellant has argued in Remarks Pg.79:

> Regarding the phrase "second bounded range", according to the specification the second bounded range represents performance parameter variations due to different device designs. This is explained in greater detailed in paragraphs [0020]-[0030] and illustrated in Figures 2-3…

(Response 18) Specification [0020]-[0030] does not include any indication of the second bound range clearly specifying it metes and bounds. The suggested curves are placeholder values which do not specify the metes and bounds. Appellant is requested to provide a clear range.

e. CLAIM OBJECTION

Examiner notes appellant's intentions regarding filing amendment under 37 CRF 1.1312.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Akash Saxena/

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